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Semiconductor Devices for the Detection of Ionising Radiation

Heidelberg Graduate School 7-10 April 2015

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Overview

- Introduction
 - Semiconductors
 - Interaction of charged particles and photons with matter
 - Charge carrier transport
- Hybrid pixel detectors
 - Application in tracking / vertexing and imaging
- Readout (electronics)
- Radiation damage and tolerance
- Active pixel detectors



- A solid state detector which is segmented into sensing elements
 - A charged particle or a gamma ray produces a signal by ionisation
 - Pulse processing electronics amplifies the signals and distinguishes signals from noise
 - Signal gives true 1- or 2-dimensional spatial information
 - i.e. the position information is not obtained by combinations of measurements (e.g. x/y, r/drift time)
 - Typical segmentation: strip and pixels (will focus on the latter)



- Different flavours of semiconductor detectors
 - Construction type:
 - Sensor and signal processing electronics in two separate chips with 1:1 cell correspondence → strips and hybrid pixel detectors
 - (Part of the) Signal processing electronics in sensor chip
 → active pixel detectors
 - Signal processing:
 - Single event readout
 tracking
 - Counting
 - Integrating

imaging



ATLAS Pixel Detector

= 1744 modules

Applications





The Large Magellanic Cloud (taken with the pn-CCD camera)







- Leonardo Rossi, Peter Fischer, Tilman Rohe, Norbert Wermes,
 Pixel Detectors, From Fundamentals to Applications Berlin, Springer 2006
- Helmuth Spieler, Semiconductor Detector Systems Oxford University Press 2005
- Gerhard Lutz, Semiconductor Radiation Detectors: Device Physics Berlin, Springer 1999 (Repr. 2007)



Introduction:

Semiconductors (mostly actually: Silicon)





- In nature Si usually occurs as silicon dioxide (quartz)
- For sensors pure crystalline silicon is used
- Silicon crystals:
 - Crystal structure: diamond lattice
 - Each atom has 4 covalent bindings to its (equidistant) neighbours
 - Lattice constant 5.43 Å
 - Energy levels of atoms form a band structure



Kay Chernush





Band gap energies E_g at room temperature:

Si 1.12 eV Ge 0.67 eV GaAs 1.42 eV Diamond 5.5 eV



- Slight temperature dependence, e.g. Si at 0K: $E_g = 1.17 \text{ eV}$
- At 0K: all states in the valence band filled, all states in the conduction band empty
- At higher temperatures: electrons can move to the conduction band, due to thermal excitation → Fermi-Dirac statistics



Electrons and Holes





valence band

- Moving an electron from the valence to the conduction band leaves an unoccupied state in the valence band = hole
- Electrons in the conduction band and holes in the valence band can be treated similar to free particles, however with a different effective mass m_n or m_p , resp.
- In the crystal this is equivalent to removing an electron from a covalent bond between two Si atoms



- Concentration of electron and holes: *n*, *p*
 - Defined by Fermi-Dirac statistics F(E) and state density N(E): $n = \int_{E_c}^{\infty} N(E)F(E)dE$
- Un-doped (intrinsic) semiconductor: n=p=:n,
- From Fermi-Dirac:

$$n \cdot p = N_C N_V \exp\left(\frac{-E_G}{kT}\right)$$
 and $n_i = \sqrt{N_C N_V} \cdot \exp\left(-\frac{E_G}{2kT}\right)$

• Example, in Si: $N_c = 2.8 \times 10^{19} \text{ cm}^{-3}$, $N_v = 2.65 \times 10^{19} \text{ cm}^{-3} \rightarrow n_i \sim 1 \times 10^{10} \text{ cm}^{-3}$



- Fermi Level E_F : from n = p follows $E_F = \frac{E_V + E_C}{2} + \frac{1}{2}kT \ln \frac{N_V}{N_C}$
- i.e. E_{F} is typ. In the centre of the band gap



Fig. 15 Intrinsic semiconductor. (a) Schematic band diagram. (b) Density of states. (c) Fermi distribution function. (d) Carrier concentration.



- The property of semiconductors can be modified by adding impurities to the lattice ("doping")
- Typically the dopants are either
 - Atoms with 5 valence electrons (donors), group V elements like phosphorous or arsenic
 → n-type silicon
 - Atoms with 3 valence electrons (acceptors), group III elements like boron
 → p-type silicon
- Typ. doping concentrations: 10¹³ cm⁻³ to 10¹⁸ cm⁻³
- Due to *n*·*p*=*const.*, increasing one type of charge carrier, the other decreases (majority and minority c.c.)





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Valence band

- Donor provides one weakly bound extra electron
- Equivalent to:
 - Additional energy levels very close to the conduction band

E,

- E_F closer to conduction band



- Acceptors leave a "broken bond" (hole) that is free to move
- Equivalent to:
 - Additional energy levels very close to the valence band
 - E_F closer to valence band



Doping Summary (1)

• Intrinsic

• n-type

• p-type





- To summarise:
 - In intrinsic semiconductors the Fermi-level is close to the middle of the band gap
 - In p-type semiconductors the Fermi-level moves towards the valence band
 - In n-type semiconductors the Fermi-level moves towards the conduction band
- Helps understanding what happens at interfaces:
 - Two sides go into thermal equilibrium
 - \rightarrow Fermi-level needs to line up



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Introduction:

Interaction of particles with matter











δ -Electrons



Measurement in a gas-filled chamber



Simulation of δ -range with (dots) and without (circles) multiple scattering







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Compton Scattering

Klein-Nishima



Condensation on the ions appears in white.



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Measured Photon Energy







- High-energy charged particles: particle passes through the detector, leaves a track of e-h-pairs with uniform density
- X-rays: Leaves a nearly point-like charge cloud. A beam of X-rays is attenuated in intensity; the absorption length depends on the energy
- Visible light and UV: same as X-rays, but with very short absorption length (typically < 1 μ m in Si), small signal
- α-particles: similar to high-energy charged particles, but with high ionisation, typically stopped after a few µm (energy dependent)
- β-particles: "between" high-energy charged particles and α-particles. Depending on energy, they can even pass through the sensor



Introduction:

Charge carrier transport







Charge Carrier Transport

Combining charge drift, diffusion and magnetic field effect:



 In a segmented detector all three effects determine the position and shape of the hit clusters



Hybrid Detectors

the most common silicon detector type!



- Doping summary:
 - In intrinsic semiconductors the Fermi-level is close to the middle of the band gap
 - In p-type semiconductors the Fermi-level moves towards the valence band
 - In n-type semiconductors the Fermi-level moves towards the conduction band
- Use to understand what happens at pn-junction:
 - Two sides go into thermal equilibrium
 - → Fermi-level needs to line up



- Difference in charge carrier concentrations leads to diffusion current across junction
- Opposite carriers recombine and lead to fixed space charges in junction region



Fig. 2.6. Schematic illustration of a pn-junction (a) and its band diagram to illustrate the formation of the built-in voltage (b)



- Generated electric field leads to drift current counteracting the diffusion current
- In thermal equilibrium: built-in voltage U_{bi} – can be calculated from lining up of Fermi levels or from space charges





pn-Junction as Detector (3)

thin, highly doped p⁺ ($\sim 10^{19}$ cm⁻³) layer on weakly doped n⁻ ($\sim 10^{12}$ cm⁻³) substrate



- Detection mechanism:
 - pn-junction under reverse bias: depleted bulk
 - Charged particle or photon can create free eh-pairs
 - Field created by external bias voltage separates e,h and causes drift
 - Charge can be measured on surface electrodes





- One electrode
 segmented into strips
 - Doping of opposite type applied to bulk: can be done with a mask
 - pn-junction in each strip: isolated strips!
- Each strip is connected to one electronic readout channel



• Strip pitch p = 10...100 μ m, provides position information of precision $\sigma \le p/\sqrt{12}$


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Strip Detectors (3)





Strip Detectors (4)

- 2D information by two layers of crossed strips
 - Two separate
 Si-devices
 - Strips in both electrodes







Strips: Ambiguities







Strips: Ambiguities







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- Segment one electrode into pixels
 - True 2D-information, no problem of ambiguities at high track densities, OK for photons
- Smaller electrode size brings other benefits
 - Lower leakage current → lower noise, better radiation tolerance
 - Lower capacitance \rightarrow lower noise
- ... but also complications
 - Large number of channels, proportional to sensor area
 - Signals of each channel needs to be processed

Pixel Detectors





Concept realised as hybrid pixel detector



pixel readout chip

Will now look at three main parts of a hybrid: sensor - readout chip - interconnection



- AC-Coupling (in particular for strip sensors)
 - (Fast) signal passes through a coupling capacitor to the electronics
 - Potential is established via bias resistor
 - Leakage current flows through the bias resistor and is not integrated
 - Bias resistor and coupling capacitor usually integrated on the sensor





- Bias resistor + coupling capacitor for each pixel is difficult
- AC-coupling not necessary in pixel detectors: leakage / pixel small
- DC-coupling:
 - Direct connection between sensor and electronics
 - Ground potential is established by readout electronics
 - Problem: testing before connection
 - Leakage current needs to be compensated by electronics





- Consider two implants: one floating, one on fixed potential (e.g. ground)
- If no (or a small) back side potential is applied both implants will be surrounded only by a small intrinsic depletion zone
- If the back side potential is increased
 - the floating implant will follow the potential
 - the depletion region of the grounded implant will grow
- If the one depletion region reaches the other, a hole current will flow from the floating to the grounded implant
- The potential of the floating implant is now determined by (not equal to) the grounded implant.



- Must test sensor for quality assurance
- Implement bias structure on segmented side, biasing all pixel implants via punch through
- Once connected toreadout, bias structure is not used any more
- I-V-curves can be done with two probe needles





- Bias voltage is applied at the back plane, pixel implants are grounded by the electronics
- Problem: the cutting edge of the sensor is mechanically damaged by the cutting and therefore conductive
- The surface between cutting edge and active area will therefore be between ground potential and the bias voltage
 - The exact value depends on the conductivity but also on environmental conditions (humidity, dust etc.)
- Two extreme cases show the consequences for reliable detector operation (next slide)





From Rossi, Fischer, Wermes, Rohe, Pixel Detectors

- First case (a): segmented side is at ground level
 - In this case the depletion zone reaches the cutting edge
 - The crystal defects inject a large leakage current into the depletion zone
- Second extreme (b): the surface adjusts to the bias potential
 - A (conductive) electron accumulation layer forms due to the positive potential, such that the bias potential reaches up to the implant
 - This leads to a high local electric field and the risk of breakdown



- Solution: guard ring structures
- Structure of several floating p⁺-rings around the active area
- The rings bias "themselves" via punch-through with a potential drop between each ring and the next
- Ideally: outer ring at bias potential, such that the space charge region does not reach the cutting edge



- Differences to microelectronics:
 - Sensor needs silicon with low doping concentration
 - Complete volume and backplane are important
- Substrate material:
 - Resistivity (N_{eff}) determines the voltage needed for full depletion
 - → high resistivity material needed
 - Most sensors are from floatzone material (alt.: Czochralski, but difficult for low N_{eff})



Sensor Production (2)

• Floatzone process

• Wafer cutting





Sensor Process Flow (Example)





9. Etch oxide openings



10. Back side aluminization



11. Front side aluminization



12. Passivation

2. Photoresist for implant

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3. Etch oxide step for alignment





From: Fischer, Rohe, Rossi, Wermes: Pixel Detectors



Sensor – Schematic and Reality





Four pixels of a CMS barrel pixel sensor



ALICE sensor wafer



- Signal processing steps in the readout chips:
 - Amplification of sensor signal
 - Hit decision
 - Hit storage / counting
 - Trigger validation (HEP)
- First two steps are always done in the pixel cell, in some designs more
 - Readout architecture depends on hit rate, trigger rate, trigger latency and geometric constraints



From: Fischer, Rohe, Rossi, Wermes: Pixel Detectors

• Transfer of hit data (single hits with timestamp (tracking) or hit counts (imaging)) to periphery, periphery serialises digital information





Integration of signal charge

- In 250 µm Si: Most probable value 19000 e, but consider charge sharing between pixels, smaller charge depositions, radiation damage
- Hit decision

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Swiss army knife: many (conflicting) requirements: fast, low noise, low power consumption





- Connection between readout chip and further electronics (and for strips: readout chip and sensor) usually done with wire bonds
 - Wires are typically made of Au, Al, Cu
 - Wire diameters range from 15 to several 100 μm
 - Two main types: ball bonding (~1970) and wedge bonding (~1960)
 - Ball bonding uses gold or copper wires and usually requires heat.
 Wedge bonding uses gold or aluminium wires and requires heat (Au) or ultrasound (Al)
 - In HEP / Imaging usually wedge bonding with AI wires is used. Typical wire diameters are in the order of ${\sim}25~\mu m$











Bump Bonding

- Connection between chip and sensor is established with bump bonds
- Process used in industry, but pitches needed in HEP are typically smaller than industry standard
- Two main process parts:
 - Bump deposition
 - Flip-chip assembly
- Bump deposition usually done on wafer-level
- Electronics wafers are thinned after bump deposition (e.g. 750 μ m \rightarrow 150 μ m)



Two main techniques in HEP:

- Electroplated solder bumps
- Indium bumps



Solder Bumps



Sputter etching and sputtering of the plating base / UBM



Spin coating and printing of Photoresist



Electroplating of Cu and PbSn



Resist stripping and wet etching of the plating base

Chip

Reflow



2µm* └──

Pb-Sn

UBM

Chip

Mag = 6.04 K X WD = 3 mm

~20-25µm

EHT = 20.00 kV

Detector = InLens

Store resolution = 1024 * 768



©VT

Date :2 Nov 2001 Time :14:08:2 VTT Microelectronics Centre

Fischer, Rohe, Rossi, Wermes: Pixel Detectors

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Alenia Marconi Systems

Indium Bumps



Alenia Marconi Systems, Rome



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- The standard In process does not include a reflow step
- One worry: small distance between readout chip and sensor could lead to noise injection
- Process used in CMS (pitch 100 μ m): Indium bumps with reflow
 - $\rightarrow\,$ distance sensor readout chip approx. 15 μm



Ch. Broennimann et al., NIM A 565 (2006) 303 – 308







What can go wrong

- Many possibilities for failures:
 - Missing or merged bumps (single dead pixels)
 - Mechanical defects, from chipped edges to broken wafers ("best" case: increase of currents, worst case: complete chips lost)
 - Incomplete removal of photo resist

(if on wire bond pads, no bonding possible)

→ Careful inspection and testing after all process steps





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- Future trends in Interconnect:
 - Smaller bump bond pitches
 - Lead free bump bonds
 - Reduce price per area
 - Reduce the number of wire bonds
 - → 3D-Integration / vertical interconnect



- Pros and Cons of Hybrid Pixel Detectors
 - + Chip and Sensor can be optimised independently (they are not produced in a common process, even different materials are possible)
 - + Fast, parallel matrix readout possible
 - + Radiation hardness
 - + Relatively large signal (~20000 e in 250 µm)
 - + Mature technology
 - Challenging interconnect technology
 - Material budget: sensor + electronics chip + cooling + support are in the active area
 - Pixel cell size directly coupled to the electronics cell size



- Example: ATLAS Pixels
 - Module made of 1 sensor tile and 16 FE chips
 - 1.6 x 6.1 mm active area
 - 328 x 144 = 47232 pixels
 - Most pixels: 50 x 400 µm² size
 - Digital readout, pulse height is measured with "time over threshold" (ToT)





ATLAS Pixel FE Cell







- Length of preamplifier (and discriminator) pulse depends on
 - Deposited charge: Used for charge measurement from ToT
 - Feedback current: Can be used to homogenise the ToT Behaviour
 - Threshold



- Full detector consists of three barrel layers and two end caps with three discs each
- 1744 modules
- ~ 2 m² active area
- 80 Million channels







Medipix



IEEE TNS 49, 5 (2002), 2279 - 2283

- Medipix 2: example of an imaging chip for hybrid pixel detectors
 - Readout logic in the pixel cell substituted by counter
 - Double discriminator for energy windowing


X-Ray Transmission Radiography



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S. Pospisil, Vertex 2006

- Medipix: X-ray transmission image of termite worker body (left) and detail of its head (right).
 - (Magnified 15x, time=30s, tube at 40kV and 70μ A)
- Soft tissue organism \rightarrow Good model to test the sensitivity



Applications Charged Particles in Tracking

Photons

in Imaging

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I) Hybrid Pixel Detectors in Tracking

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- Measure trajectory of charged particles
 - Measure several points along the track and fit curves to the points (helix)
- Extrapolate tracks to the point of origin
 - Determine positions of primary vertices and identify interesting collision vertex
 - Find secondary vertices from decay of long-lived particles (lifetime tagging)
- Use the track curvature to determine the particle momentum



Primary vertices





 Tracks from secondary vertex have significant impact parameter with respect to primary vertex

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Example of a fully reconstructed event from LHCb with primary, secondary and tertiary vertex



- Spatial resolution
 - Single point resolution
 - Double track resolution
- Efficiency (100%) / Noise
- As little material as possible
 - Multiple scattering
 - Photon conversion
- Time resolution
- Radiation hardness



• Simple case: Two tracking layers / measurement points $d_{1/2}$ at radii r_1 and r_2 , extrapolation to r = 0





• Error propagation:

$$\sigma_{d_0}^2 = \frac{r_2^2 \sigma_{d_1}^2 + r_1^2 \sigma_{d_2}^2}{(r_2 - r_1)^2}$$



$$\sigma_{d_0}^2 = \frac{r_2^2 \sigma_{d_1}^2 + r_1^2 \sigma_{d_2}^2}{(r_2 - r_1)^2}$$

- Error of inner point is weighted with outer (larger) radius
 → Spatial resolution of inner layer particularly important
- For equal resolutions:

$$\sigma_{d_0}^2 = \frac{r_2^2 + r_1^2}{(r_2 - r_1)^2} \sigma_d^2 \\ \left(\frac{1}{(1 - r_1/r_2)^2} + \frac{1}{(r_2/r_1 - 1)^2}\right) \sigma_d^2$$



- Tracker design:
 - Vertex resolution suggests to make the inner radius as small as possible and the outer radius as large as possible
 - Limit 1 (Inner radius): Beam pipe, track density, radiation damage
 - Limit 2 (Outer radius): Cost



- Additional contribution due to multiple scattering $\theta_0 = \frac{13.6 \text{ MeV}}{\beta cp} z \sqrt{x/X_0} \Big[1 + 0.038 \ln (x/X_0) \Big]$
- For a track with $\theta \neq 90^{\circ}$: $r \rightarrow \frac{r}{\sin \theta}$, $x \rightarrow \frac{x}{\sin \theta}$
- This results in:



Constant term depending on geometry, term depending on material, decreasing with p_{τ}



S.Alekhin et al. HERA and the LHC - A workshop on the implications of HERA for LHC physics:Proceedings Part B, arXiv:hep-ph/0601013.

- CMS/ATLAS:
 - 20µm @ 20 GeV
 - 100µm @ 1 GeV
- ALICE better resolution in particular at low p_τ, due to less material





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Single Point Resolution

- Simplest example: 100% single hits; Only the pixel containing the track fires, independently of the track position inside the pixel
- Reasonable assumption: particle passage was in the middle of the hit pixel
- Reconstruction error depends on the true position of the track
- Assuming tracks are equally distributed over the width of 1 pixel: *residual distribution* is box distribution with width equal to the pixel pitch





• Close to the pixel boundary charge will spread over two pixels and cause a hit in both pixels

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- Reconstruction: assume centre between two pixels
- One can consider the residual distribution as the sum of two box distributions; one for double and one for single hits
 - Their widths depend on the width of the region around the pixel border that creates double hits
 - Nicely visible if the diffusion width is much smaller than the pixel size (example: 400 µm direction of ATLAS pixels)
 - Of course in reality the edges are smeared with the diffusion profile)





- Reconstruction error = std. deviation defined by probability distribution
- For a normalised box distribution centred around 0, with width p, this yields: $1^{\frac{p/2}{2}}$

$$\sigma_x = \sqrt{\frac{1}{p} \int_{-p/2}^{p/2} x^2 dx} = \frac{p}{\sqrt{12}}$$

(note: by construction this is not a Gaussian error, e.g. strictly speaking there will not be 68% of the data within 1σ around the mean)

- This is what is usually quoted as resolution with binary readout; the value improves with double hits
 - Optimal value: 50% double hits in principle halves the pixel size



- Improve resolution with pulse height information
- Simplest method: linear interpolation, using the charge deposited in the edge pixels of the cluster:

$$\Omega = \frac{q_{last}}{q_{first} + q_{last}}$$

 The hit position is reconstructed from the geometrical centre of the cluster and Ω:

$$x = x_{centre} + \Delta_x \left(\Omega_x - \frac{1}{2} \right)$$

with Δx calibrated from data (plotting the residual vs. the charge sharing)





- Standard method in strip detectors: η-algorithm
- Use the signal of the two highest pixels S_{left} , S_{right} and define

$$\eta = \frac{S_{left}}{S_{left} + S_{right}}$$

- η values range from 0 to 1; values are typically distributed non-uniformly
- Assuming the track positions are uniformly distributed, one needs a transformation from the measured η-distributions to a uniform distribution. This is given by integration of the measured η-distribution

$$f(\eta_0) = \frac{1}{N} \int_0^{\eta_0} \frac{dN}{d\eta} d\eta$$

• For a measured value η_0 the corrected hit position is $x = x_{left} + p \cdot f(\eta_0)$



II) Hybrid Pixel Detectors in Imaging

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- Hybrid Pixel Detectors in Imaging
 - Useful energy range for Si: $\sim 4 35$ keV
 - Large dynamic range with linear response
 - Low contrast detectability \rightarrow Possible dose reduction
 - No sensitivity to dark currents → no dark frame correction necessary (and allows for measurements with low intensity and long exposure time)
 - High maximum count rates possible, allows for high intensity measurements



- Pixel detector in counting mode measures an intensity profile which can be used to calculate the absorption
- Absorption depends on
 - Radiation type and spectrum
 - Object composition and density
- Possible sources:
 - X-ray tube
 - Synchrotron radiation
- Tomography: rotate object and prepare 3D-image from 2D-projections





 Spatial resolution in imaging can be characterised by the point spread function *PSF*, i.e. by the image intensity *I* for a point-like object

$$O_0(x,y) = \delta(x,y)$$

• In a linear system the image of an arbitrary object *O* is a convolution $I(x,y) = (O*P)(x,y) = \int_{-\infty}^{+\infty} \int_{-\infty}^{+\infty} O(x',y')P(x-x',y-y')dx'dy'$

Where P is the point spread function:

$$PSF(x,y) = (O_0 * P)(x,y) = \int_{-\infty}^{+\infty} \int_{-\infty}^{+\infty} \delta(x',y') P(x-x',y-y') dx' dy' = P(x,y)$$



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Test of Spatial Resolution



S. Pospisil/Prague

Illuminating detector with known pattern ullet



- A pixelated system samples the image with a certain frequency which gives the problem of aliasing
- This can be avoided by "oversampling" with an angulated slit: putting the slit under a small angle w.r.t the segmentation yields several measurements with a slightly shifted phase



- Uniform object does not necessarily result in a uniform image
 - Example from photography: vignetting
- Main problem in imaging: pixel-to-pixel variations of the threshold can change the count rates
 - For low energies or
 - When charge is split between several pixels (threshold variations effectively change the pixel size)
- Flat field correction: take image with uniform illumination to obtain correction factors for each pixel
- Since the efficiency is energy dependent, this needs to be done for the same energy as the real exposure



• Beam hardening: When polychromatic X-rays pass through an absorber, the soft part of the spectrum is absorbed more strongly

 \rightarrow the higher the traversed absorber thickness the harder the spectrum

- Problem: The pixel efficiency is energy dependent
- Due to beam hardening the flat field correction needs to be done for different amounts of absorber



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Beam Hardening Calibration



IEAP, Czech Technical University, Prague

- The flat field correction has to be done with several absorbers of different thickness
- Absorber thickness should cover the range of the object to be inspected



Example: Flat Field Correction and Beam Hardening

Flat field correction by open beam image



Flat field correction by image of 0.16mm Al foil



Daisy blossom

IEAP, Czech Technical University, Prague

- Left: flat field correction done without absorber noise in dark regions
- Middle: flat field correction done with 0.16 mm Al noise in bright regions
- Right: flat field correction adapted according to the measured attenuation



- Considerations for imaging readout chips:
 - Change triggered readout to single photon counting (using a shutter)
 - HEP pixels have the wrong shape (usually rectangular for momentum measurements in a magnetic field) → move to quadratic
 - Chips for HEP applications (in particular their analogue parts) are usually tailored to high ρ Si and one charge carrier type. For imaging one should foresee use of other materials and both carrier polarities
- Some newer developments:
 - Allow charge summing of several pixels around the hit one to improve spectroscopic performance (Medipix 3)
 - Perform photon counting and charge integrating simultaneously in each pixel (CIX)



Crystallography - PILATUS

Pixel Detectors for Protein Crystallography



Ch. Brönnimann / PSI



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Crystallography - PILATUS

PILATUS chip architecture: Single photon counting electronics



Ch. Brönnimann / PSI



- Pilatus detector system for x-ray crystallography
 - Here: Pilatus 6M with
 ~6 million pixels
 - Total active area:
 424 x 435 mm²
- Pilatus chip:
 - Fast counting chip with 20 bit dynamic range
 - Count rate up to 1.5 MHz / pixel



PSI Villigen



Crystallography - PILATUS



Thaumatin crystal

Data Taking:

Data set: 120° Exp Time: 4s Integration: 1° Beam energy: 11.9 keV Beam intensity: 13.5% D Sample-Det: 128 mm Resolution: 1.4 Å

Analysis:

3 data sets merged full geometrical correction Processed with XDS

R_{obs}: 8.9% (overall) Completeness: 90% (98% up to 1.6 Å)

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Readout

(signal formation & electronics)

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Small Pixel Effect





CMOS Amplifier








- Thermal noise
 - Thermal fluctuations of electron distribution
 - From thermodynamics: noise power spectrum in a resistor R:

$$\frac{\overline{\mathrm{d}U^2}}{\mathrm{d}f} \equiv e_n^2 = 4kTR$$

- Ideal resistor with serial voltage noise source or parallel current noise source $\frac{1}{12}$

$$\frac{\mathrm{d}I^2}{\mathrm{d}f} \equiv i_n^2 = \frac{4kT}{R}$$

- "white" noise, i.e. independent of frequency

 (i_{n^2} / e_{n^2}) often used to denote spectral current / voltage noise densities)



- 1/f-noise
 - Various sources depending on the component

$$\frac{dU^2}{df} \approx \frac{A}{f^{\alpha}} \quad \text{with} \quad \alpha \approx 1$$

- 1/f behaviour is observed when noise sources include several processes with different time constants
 - E.g.: trapped charges that are released with different time constants depending on the trap depth



- Shot Noise:
 - Shot noise is due to the discrete nature of charge
 - Consider a current I in a short time interval Δt
 - The number of electrons crossing a boundary along the current path is given by $\Delta N = \frac{I\Delta t}{\Delta t}$

$$\Delta N = \frac{n\Delta t}{e}$$

- Statistical fluctuation in the number of charge carriers:

$$\delta \Delta N = \sqrt{\Delta N}$$
$$\Rightarrow \left\langle \delta I^2 \right\rangle = \frac{e^2 (\delta \Delta N)^2}{\Delta t^2} = \frac{e^2 \Delta N}{\Delta t^2} = \frac{eI}{\Delta t}$$

- Spectral density: $i_{n^2} = 2Ie$



- N.B.: Shot noise requires the charge carriers to be independent of each other
- Also, shot noise (differently than thermal noise) requires a current caused by an external voltage; thermal noise is present even without an external voltage



- The output noise has to be set into relation with a typical signal amplitude.
- Raw noise values (rms output voltage) are
 - Difficult to interpret
 - Difficult (impossible) to measure
- Use equivalent noise charge ENC

 $ENC = \frac{output \text{ voltage (rms)}}{output \text{ voltage for input charge of 1e}}$

 Interpretation of noise values is now straightforward, measurement is easily possible if a calibrated charge deposition (injection) is possible Total ENC filtered by shaping (time constant τ) has three contributions

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- Different dependence on the shaping time constant (const, $\sim \tau$, $\sim 1/\tau$)
 - → Noise as a function of the shaping time has a minimum / there exists an optimal shaping time
- Two of the contributions increase with increasing sensor capacitance, the third one with increasing leakage current
 → Advantage of pixel detectors w.r.t. strip detectors, as both are much smaller





Radiation damage and tolerance

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Classification of Defects



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Displacement Damage Cross Section





Leakage Current



- Increase in leakage current:
 - Normalised to volume V: independent of Si-type
 - Depends linearly on fluence
 - Clear annealing effects



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Effective Doping Concentration (1)



- No. of acceptor-type states increase with fluence
- When starting n-type: type-inversion





annealing time at 60°C [m in]

 Also annealing effect here, but in addition reverse annealing



- n-in-n sensor
 - n-in-p after type inversion, allows underdepleted operation (next slide)
 - Reminder: voltage needed for full depletion increases for large fluences
 At some point it might not be possible to fully deplete the sensor
 - Pixels need to be isolated from each other
 - Several possibilities:
 - P-stop: localized high-dose p-implant
 - P-spray: low-dose p-implant over the full surface
 - Criteria: avoid high local electrical fields that could lead to breakdown; consider situation before and after irradiation



Different Sensor Options

p-Pixel on n-Substrate

n⁺-Pixel on n-Substrate



 After type inversion p-in-n (then p-in-p) sensors can be operated only fully depleted; otherwise pixels are short-circuited



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Moderated p-spray



From Rossi, Fischer, Wermes, Rohe, Pixel Detectors

- Use two-step profile in the doping concentration: a higher concentration to guarantee the isolation and a lower concentration close to the n+-implant to reduce the maximum electric field
- Good high-voltage stability before and after irradiation
- Profile can be obtained by changing the process order: do p-spray implant after the adding e.g. the nitride layer (which is there anyway) → no additional mask step



Example Defect Engineering



- Measure energy levels in band gap, e.g.:
 - Thermally Stimulated Current (TSC) charge injected cold → heating under bias → charge released when T corresponds to E-level



- Trapping time describes loss of signal
- Trapping time inversely prop. to fluence, little material dependency



Charge Movement in MOS





I) Radiation Damage in Electronics



- Radiation damage effects in electronics
 - Oxide charges lead to threshold shifts in MOSFETs
 - For thick oxides (thickness > 12 nm) density of created interface states depends by a simple power law on oxide thickness
 - For thin oxides (thickness < 12 nm) density of interface states is significantly below this power law (explanation: tunneling)
 (see IEEE TNS, Vol. 33, No. 6 (1986)1185 1190)
 - Improvement in this effect comes "for free" by deep submicron technologies (e.g. gate oxide thickness in .25 µm: ~ 5 nm)
 - Oxide charges lead to conducting channels between drain/source of a transistor and between neighbouring transistors
 - Radiation-induced change of charge carrier mobilities changes transistor parameters (transconductance)



- Standard technology: use annular transistors with guard rings to suppress leakage current
 - No leakage current path from source to drain without passing the (annular) gate
 - Difficulties: Need to develop own design rules and transistor models





II) Pixel sensors for high fluences

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II a) 3D pixel sensors for high fluences

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- 3D technology:
 - Electrodes are not on the sensor surface but are processed nearly through the entire bulk
 - Electrodes are made by etching
 holes in the silicon bulk; the
 borders of the hole can be
 doped with dopant gases and
 filled with polysilicon
 - Originally proposed to solve trapping-problem in GaAs sensors, turned out to be one possibility to increase the radiation hardness of Si sensors





3D-Pixel Sensors



- 3D-architecture decouples electrode distance (drift length, depletion region) from device thickness (total signal / absorption probability)
 - Shorter drift path \rightarrow faster charge collection
 - Lower voltage for full depletion



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- Vertical electrodes are connected on the sensor surface to form the electrodes for biasing and readout
- Many different segmentation types implemented by now:
 - **Strips**
 - **Rectangular pixels**
 - **Quadratic pixels**
- Connection to the electronics like for a planar sensor



Nucl. Instr. and Meth. in Phys. Res. A 531 (2004) 56-61





Double-Sided 3D





- Two different approaches:
 - Etch all electrodes from one side only or n- and p-type from different sides



- Measurement of signal efficiency vs. fluence for different geometries
 - Signal efficiency: ratio of average signal at a given fluence devided by the preirradiation value
 - 50% or more signal efficiency at 1 x 10¹⁶ n_{eq} cm⁻²
 100% signal defined by sensor thickness



ATLAS IBL Technical Design Report, CERN-LHCC-2010-013



Inefficient Regions



- One problem of 3D sensors: column electrodes are dead regions
- But only a problem for exactly perpendicular tracks





- P. Hansson, et al., Nucl. Instr. and Meth. A (2010), doi:10.1016/j.nima.2010.06.321 The 3D technique can be used to implant a deep trench around the active area which acts as bias electrode and terminates the depletion region before the cutting edge
 - Advantage: less dead area than for a multi-guardring structure ("active edge" sensors) Here: sensor active up to 6 µm from the cutting edge





II b) Planar pixel sensors for high fluences

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- Alt. to 3D-approach: faster charge collection by achieving maximum possible electric field
- How to increase the electric field? \rightarrow increase the bias voltage
- Problem: even if the sensor does not break through, often the services cannot deliver much higher bias voltages
- But:
 - <E> = U/d
 - At high fluences, large d does not increase the signal (trapping)
 - → Go for thin sensors:
 higher average field at same bias voltage,
 less strongly peaked weighting field



- Which sensor types to use:
 - We want electron collection (faster charge collection, less trapping), therefore we have to use n-side readout, i.e. n-type pixels on n- or p- substrate
 - p-on-n is in addition ruled out by type inversion
 - Both remaining options are currently investigated, e.g. for HL-LHC
 - n-on-n: like current LHC detectors; has proven to work...
 - n-on-p: no type inversion, p-n-junction is always on the pixelated side

 \rightarrow can be done in a single-sided process, with the guard rings on the readout side

Difficulty: a large fraction of the bias voltage is present close to the electronics; together with the need for high bias voltages this requires a strong, high-quality passivation on top of the normal oxide



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Signal Charge vs. Fluence



ATLAS IBL Technical Design Report, CERN-LHCC-2010-013

- Charge collected in 300 μ m sensors at 900 V
 - At 5 x 10¹⁵ n_{eq} cm⁻²: ~ 8000 e
 - Still possible to detect with low-noise electronics







ATLAS IBL Technical Design Report, CERN-LHCC-2010-013

- Comparison of different sensor thicknesses vs. bias voltage
 - Higher signal in the thinner sensor as expected





- At high electric field the charge exceeds the expected signal ... and even the total deposited charge
 - Suspected effect: charge multiplication in the high-field regions close to the collecting electrodes. Currently under study...


(Semi-)Active Pixel Detectors



- p+-p and n+-n junction:
 - Also for same-sign doping the concentration difference leads to a diffusion current and therefore a space charge
 - The built-in potential can be calculated from the difference of the Fermi-levels. The direction is such that, when going from lower to higher doping, minority carriers see a potential barrier of height

$$V = \frac{kT}{q} \ln \frac{N_+}{N}$$

 Thermally moving charge carriers (E=3/2 kT) will be reflected at the barrier
(N₊ and N₋ differ by several orders of magnitudes)



After: Lutz, Semiconductor Radiation Detectors





- Charged particle generates electron hole pairs in the epitaxial layer
- Electrons move by diffusion; they are reflected by the substrate and the p-wells and eventually reach the collecting n-well
- Small depletion region around n-well; complete charge collection only here



- In-pixel electronics: simplest form: 3 transistors: source follower, reset and select switch
- Of course also more electronics possible (shaper, discriminator)
- Design complication: in the pixel usually only one type of MOSFETs possible
 - The n-well of a pMOS would collect charges
 - No real CMOS circuitry possible







G. Anelli





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Matrix Readout (MIMOSA Family)





- Charge collection does not depend on full depletion, no electric field
- Main effect of radiation damage:
 - Defect states in band gap lead to decrease of charge carrier lifetime
 - Decrease in charge collection efficiency
 - Decrease of S/N and therefore detection efficiency (and resolution)
- Main reason for the radiation damage is the slow charge collection; improvements in the charge collection speed would therefore reduce the sensitivity to trapping
 - High resistivity epi-layer
 - High voltage? (see later)



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MAPS in High Resistivity Epi Layer











- Use of commercial CMOS processes
 - Low cost, but dependence on availability of suitable commercial processes
- Signal processing integrated on sensor \rightarrow compact, no bump bonding
- Very small pixel sizes possible; spatial resolution can be below 5 μ m
- Charge is collected in the epitaxial layer
 - Typical thicknesses up to ~ 15 μ m \rightarrow charge < 1000 e / low X-ray efficiency
 - Low noise electronics needed
 - Chip can be thinned down as most of the thickness is not needed for signal
- Small depletion zone around n-well
 - Usually incomplete charge collection
 - Collection by diffusion: slow signal development (~ 100 ns)
- Less radiation hard and slower (for tracking) than hybrid pixels



- Size of pixels is limited due to charge collection; electrode distance should not be too large
 - Motivation would be power consumption (if extremely high spatial resolution is not needed, lower channel density would result in lower power density)



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• Examples

500-fps, 1.3-Megapixel CMOS Image Sensor

Featuring Micron's TrueSNAP[™] Electronic Shutter



- 1,280H x 1,024V image resolution
- TrueSNAP[™] freeze-frame electronic shutter
- 500 frames per second (fps)
- Monochrome or color digital output
- <500mW maximum power dissipation @ 500 fps
- On-chip, 10-bit analog-to-digital converters (ADCs)
- Simple digital interface

Description

Micron's MI-MV13 is one of the industry's fastest CMOS image sensors. It features Micron's revolutionary TrueSNAP freezeframe electronic shutter, which enables simultaneous exposure of the entire pixel array to stop even the fastest motion with crystal clear images. It delivers 10-bit color or monochrome digital images with a 1.3-megapixel resolution at 500 fps—or 655 million pixels per second—for machine vision and high-speed imaging applications.

Applications

The MI-MV13 CMOS image sensor captures complex high-speed events for traditional machine vision applications as well as various high-speed imaging applications. Its electronic shutter is capable of freezing and capturing near-instantaneous events with a 1.3-megapixel resolution while outputting 500 fps. The sensor can capture an event with a series of images taken at a high repetitive rate, enabling them to be viewed at lower speeds.

Applications include machine vision (production line monitoring and control for industries ranging from semiconductor fabrication to food sorting), automotive testing, microscopy, traffic control, 3D imaging, animation, motion analysis, film special effects, forestry, industrial and military research, and security systems. The MI-MV13's capabilities enable camera performance far beyond current CCD-based systems, creating





- MIMOSA-26 (<u>Minimum Ionising Particle MOS Active</u> Pixel Sensor)
 - 0.35 µm process with high-resistivity epitaxial layer
 - Column parallel architecture; in-pixel amplification, end-of-column discrimination
 - 1152 x 576 pixels, pitch 18.4 μm (active area: 21.2 x 10.6 mm²)
 - Charge sharing $\rightarrow \sigma \sim 4 \ \mu m$
 - Readout time ~ 100 μ s (10⁴ frames/s)
 - ~250 mW/cm² power consumption





Marc Winter, IPHC, Strasbourg



MAPS Beam Telescope

- EUDET Beam telescope
 - 2 arms of 3 planes each
 - MIMOSA-26 thinned to 50 µm
 - Used for sensor tests in several test beams at CERN and DESY
 - Extrapolation error ~ 1-2 μm even with 3 GeV e⁻ (DESY)
 - Frame readout frequency O(10⁴)Hz



Marc Winter, IPHC, Strasbourg



STAR Heavy Flavour Tracker



STAR Collaboration

- Direct reconstruction of charm; detection of charm decays with small ct, including $D^{\scriptscriptstyle 0} \to K\pi$
- Resolve displaced vertices (100 150 microns)
- \leq 30 µm IP resolution required for 750 MeV/c pion
 - Pixel size \leq 30 µm, material as low as possible, should be below 0.5% X₀/layer (goal: 0.37)





- 2 Innermost layers (r = 2.5, 8 cm): MAPS Pixels thinned to 50 μ m
- Air cooling (power dissipation ~ 170 mW/cm²)
- Ladders made out of 10 MAPS chips



Stitched Sensors

- Variation 0: stitching
- Standard CMOS limited to 2.5 x 2.5 cm2
- Some foundries offer stitching
 - Relatively new technique
 - Allows to produce wafer scale chips
- Here: LAS (Large area sensor) for imaging
 - 5.4 x 5.4 cm2
 - For x-ray imaging (with CsI:Tl scintillator grown on a fibre-optic plate)
 - Large dynamic range (and large size) allows simultaneous diffraction and transmission imaging



Few 100µm Substrate



• Variations I: The INMAPS Process





How much CMOS in a CMOS Sensor?



Renato Turchetta

- 100% efficiency \rightarrow only nmos in pixel \rightarrow no complicated electronics
- Complicated electronics \rightarrow nmos and pmos, i.e. cmos \rightarrow low efficiency





- Standard CMOS with additional deep p-well
- 100% efficiency and CMOS electronics
- Optimise charge collection and readout electronics



60

50

40

30

20

10

% total signal

-10

- Laser scan in pixels with and without deep p-well (DPW)
- Simulation and measurement show improved charge collection with DPW





M. Stanitzki, Pixel 2010

10

30

Position in cell (microns)



- Variations II: High-Voltage CMOS (I. Peric et al., previously Heidelberg University)
 - The standard application of high-voltage CMOS processes is the combination of standard CMOS logic and special transistors, which can generate high output voltages, e.g. to steer electric motors or LCD displays
 - Idea: use a high-voltage CMOS process to build CMOS pixel sensors





- I. Peric, Pixel 2010
- Twin well structure; allows implementation of NMOS and PMOS transistors





• Deep well can be biased at high voltages with respect to the psubstrate; transistors inside the well will "see" only low voltages



Biasing HV-CMOS



- Expected depletion depth at 100 V bias: 14 µm
 - Mip: ~ 1000 e



Radiation Tolerance



- After p-irradiation to 10¹⁵ n_{eq} cm⁻²
 - 40 e noise at -10 deg C
 - Still good S/N for βs from ²²Na (1.567 MeV)



- Advantages:
 - Full CMOS capability
 - Fast charge collection \rightarrow advantages for radiation hardness
 - Standard industrial process
- Full readout:
 - Little room for full digital processing (limited by active area)
 - Worry of analogue digital cross-talk
 - Solution: keep digital readout separate like for hybrid detectors, but use cheap interconnect methods



Full Detector Concept (2)

Interconnection
via e.g. glue –
simple capacitive
coupling is
sufficient

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CMOS prototype with

Pixel readout chip (FE-chip)

ATLAS readout chip

Aim: wafer-to-wafer bondig



- Silicon on Insulator:
 - Try to combine the advantages of on-sensor electronics with a completely depleted sensor



- Buried oxide (BOX) separates electronics layer from active sensor volume
- Contacts through the BOX are made with vias, e.g. to the p+- pixel implants
- High resistive substrate with full charge collection and full CMOS circuitry
- Manufactured from two separate, bonded wafers
 - Not yet industry standard





Process	0.2μm Low-Leakage Fully-Depleted SOI CMOS (OKI) 1 Poly, 4 (5) Metal layers, MIM Capacitor, DMOS option Core (I/O) Voltage = 1.8 (3.3) V
SOI	Diameter: 200 mm φ , Top Si : Cz, ~18 Ω -cm, p-type, ~40 nm thick Buried Oxide: 200 nm thick Handle wafer: Cz 、 ~700 Ω -cm (<i>n-type</i>), 650 μ m thick
Backside	Thinned to 260 μ m and sputtered with AI (200 nm).



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• Complications in SOI-Sensors:

- Back-gate effect: the threshold voltage of transistors is influenced by the depletion voltage; the higher the substrate voltage the larger the threshold shift
 - \rightarrow design precautions, e.g. floating guard rings around transistors
- Radiation damage: the BOX is sensitive to ionising damage, which leads to a positive oxide charge and an increase in the transistor leakage current
 - The effect is stronger for a depleted sensor because the strong field across the oxide separates the generated charge carriers and thus reduces immediate recombination (Note: this is generally true for oxide damages; the extent of the damage depends on the bias conditions, e.g. in electronics chips it depends on whether the electronics is operated or not during irradiation)



• Current fields of development:

- Deep n-wells and deep p-wells
 - Reduce back gate effect
 - Reduce crosstalk between electronics and sensor
- Thinning
- FZ SOI wafers \rightarrow lower depletion voltage
- Double SOI wafers
 - Additional SOI structure with middle-layer bias to reduce effect of oxide charges (shield sensor from readout)
- Many different pixel chips produced (see next slide)



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SOI Chips



Y. Arai, Pixel 2010

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- Extend SOI-idea: 3D-integration:
 - Several tiers of thinned semiconductor layers interconnected to form a monolithic unity
 - Different layers can be made in different technologies
 - Industrial process!






- 3D-integration post-processing:
 - ICV =Inter Chip Vias, TSV= Through Silicon Vias
 - Hole etching and chip thinning via formation with W-plugs $\rightarrow 2.5\Omega$ per via





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Overview of Pixel Concepts



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